14.1 RTL-based Clock Recovery Architecture with All-Digital Duty-Cycle Correction

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RTL-based IP has the advantage of ease of adaptation to new silicon technology. It can be implemented by using standard hardware description languages (HDL), which are inherently independent of process and supply voltage. However, the implementation of conventional high-speed clock data recovery uses analog technology with a full-custom design flow because an RTL-based PLL [1] will lose lock in CDR applications due to frequency variation induced by power supply noise of only a few percent, with the result that RTL-based PLL architectures are not applied in real systems. An RTL-based CDR is designed and applied to a DVD system, in which substantial noise is induced by, digital circuits contained in the SoC, servo-motor and pick-up head. Experiments show that this design achieves a 496Mb/s data rate in a real operational system. Moreover, this design offers direct digital phase shift capability with 20ps resolution for generating recording write pulse sequences and an all-digital duty-cycle correction feature for generating 50% duty cycle.

Figure 14.1.1 shows a prior RTL-based PLL [1]; an RTL-based PLL must use an inverter-based digital controlled oscillator (DCO) because only inverter-based circuits can be synthesized by using standard HDL. However, inverter-based circuits do not offer immunity from power supply variations. For example, if the frequency of a DCO is 200MHz, the frequency variation will be 20MHz when the power supply is varied from 1.8V to 2.0V. This frequency error will accumulate to result in large jitter because a DCO behaves as an integrator. Behavioral simulation results show that an RTL-based PLL will lose lock in CDR applications due to frequency variations induced by only 1% power supply noise at 400Mb/s data and 400kHz loop bandwidth. Whereas, the same delay variation of our inverter-based circuits will not accumulate to result in losing lock because phases are accumulated by using a digital accumulator [2] instead of a voltage-controlled oscillator (VCO) as in a conventional CDR design.

Compared to the prior art [2] shown in Fig. 14.1.2, the strength of the design presented here includes: 1) Process portability: The implementation of the architecture is independent of supply voltage and the process because this inverter-based design (described by HDL) does not require any analog components. The prior publication [2] used an analog delay-locked loop which cannot be described using standard HDL. 2) Twice the usable operation frequency without using an analog PLL: In [2] the highest output clock, with 50% duty cycle, is obtained by dividing the clock by two, thus reducing the highest usable output frequency and as a result an analog PLL is needed to double the frequency to achieve 16X DVD read/write. In the present design, an all-digital duty-cycle correction technique is used without dividing the clock by 2, thus the highest DVD read speed of 496Mb/s is achieved without using analog components. 3) Direct digital phase shift capability with 20ps resolution for generating recording write pulse sequences.

Figure 14.1.3 illustrates the functional blocks of the RTL-based CR design. The NCPO in Fig. 14.1.2 is replaced by a fractional divider and a digital calibration delay locked loop (DCDLL), which comprises a calibration loop and a free-running digital delay line. The function of the DCDLL is to transform the digital phase generated by the fractional divider into a clock in the time domain.

The detailed operation of the DCDLL algorithm is described as follows: the digital calibration loop performs online calibration to evaluate the number of delay cells, which is equal to the period of the reference clock T. The digital multiplier multiplies the input binary code generated by the prior calibrated value, then the output of the multiplier selects one of the phases generated by the digital delay line to synthesize output clock. Consequently the digital phase generated by the fractional divider is transferred into the time domain with a resolution of one delay cell which is equal to 20ps in the present design.

Figure 14.1.4 illustrates the block diagram of the digital calibration loop and digital delay line. The digital calibration loop comprises a dummy digital delay line, a calibrated digital delay line, a digital phase detector and an up-down counter. The unit cell of the digital delay line consists of two buffers with different loading, which is implemented by adding an inverter at one of the buffer outputs as shown in Fig. 14.1.4 and a multiplexer controlled by signal D_i. When D_i is asserted, the input signal passes through the buffer with heavier loading, otherwise it passes through the buffer with lighter loading, thus the delay is only dependent on the timing difference of the propagation delay between two buffers with different loads. It should be emphasized that the resolution is not limited by that of a single inverter delay for a specified process and only depends on the skew between buffers. In our design, the resolution is typically 20ps.

The calibration loop operates as follows: A digital phase detector compares the rising edge of the dummy digital delay line output, which controls whether the signal D_i is set to zero, and the rising edge of the calibrated delay line. With the Updn_ctrl signal generated by the digital phase detector, the up-down counter decides which phase in the calibrated digital delay line is to be compared depending on the phase relationship represented by Updn_ctrl signal. Eventually, the output of the up-down counter is locked, continuously tracking temperature and voltage variation.

Figure 14.1.5 shows the block diagram of the all-digital duty-cycle correction and the programmable digital phase shift circuits. Signals with phase 0 and phase 180 are represented in the digital domain and the DCDLL transfers them into clocks in the time domain, then the rising edges of the two clocks are combined to obtain 50% duty cycle clocks. In the digital domain, the signal PCW (period control word) represents the period of the output clock and PCW/2 represents half of a period. The signal representing phase 180 is obtained by simple addition of the signal representing phase 0 and PCW/2. By using two DCDLLs, the digital phases are transferred into clock signals in the time domain; and an RS-latch is used to combine those two clocks to obtain a 50% duty cycle clock. Using the same principle, the arbitrary phase shift can be obtained in the digital domain and transferred into a pulse in the time domain.

Figure 14.1.6 illustrates that the design can directly program the phase shift of the output clock with 20ps resolution (the random jitter is filtered by the scope). Figure 14.1.7 shows the chip micrograph. This chip is implemented in a 0.13μm CMOS process. The area of the CR loop is only 0.08mm^2 and the power consumption is 5.5mW at a channel bit rate of 478Mb/s and a 1.2V supply voltage for both read/write operation. The power is about 1/4 of that reported in [2].

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References:
[1] Ching-Che Chung, and Chen-Yi Lee, "An ALL-digital Phase-Locked Loop for High-Speed Clock Generation," *IEEE J. Solid-State Circuits*, vol. 38, pp. 347-351, Feb., 2003.
[2] Ping-Ying Wang, et al., "DLL-based Clock Recovery in a PRML Channel," *ISSCC Dig. Tech. Papers,* pp. 570-571, Feb., 2005.

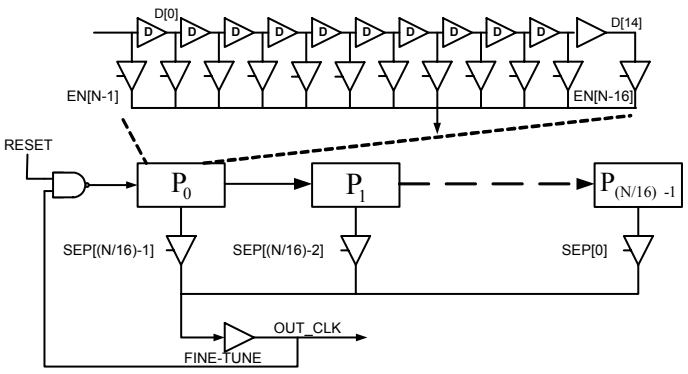

Figure 14.1.1: Block diagram of a conventional digital control oscillator [1].

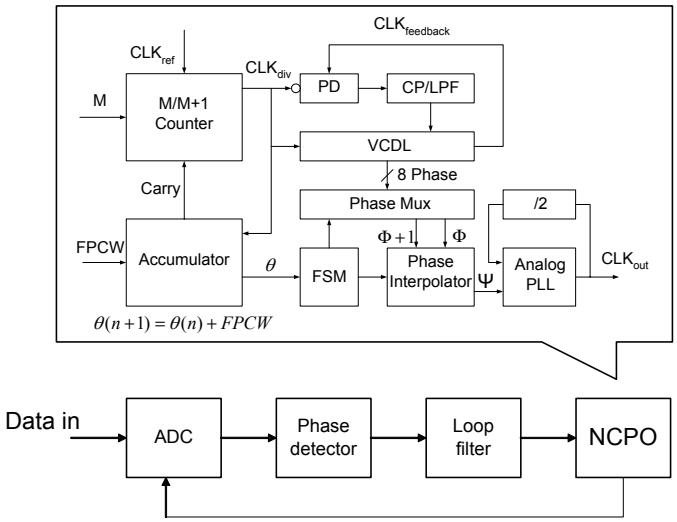

Figure 14.1.2: Block diagram of prior CDR for PRML [2].

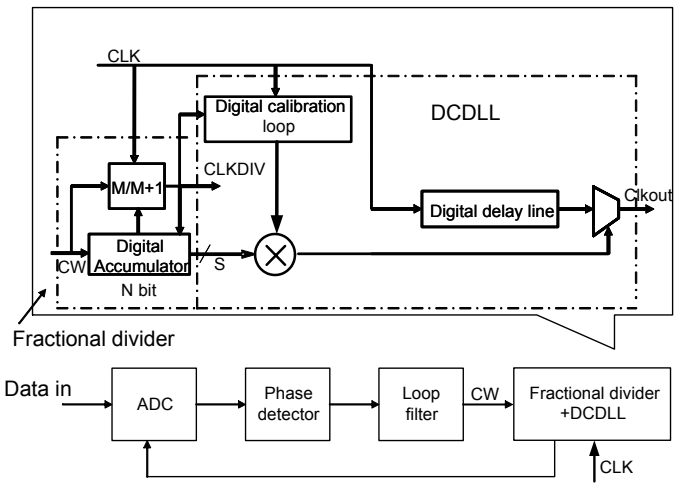

Figure 14.1.3: Block diagram of the RTL-based CR.

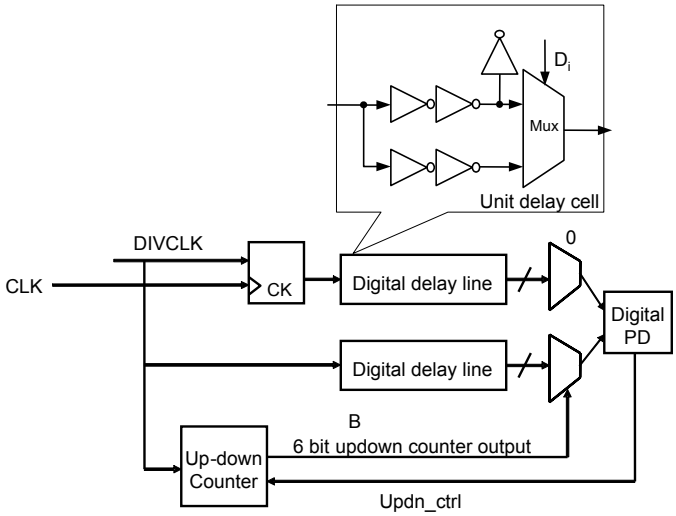

Figure 14.1.4: Block diagram of digital calibration loop and schematic of unit delay cell in DCDLL.

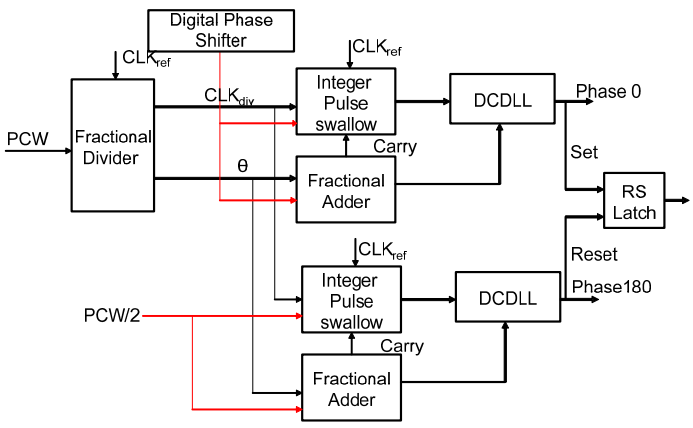

Figure 14.1.5: Block diagram of all-digital duty-cycle correction.

Figure 14.1.6: Measurement result for programmable phase shift.

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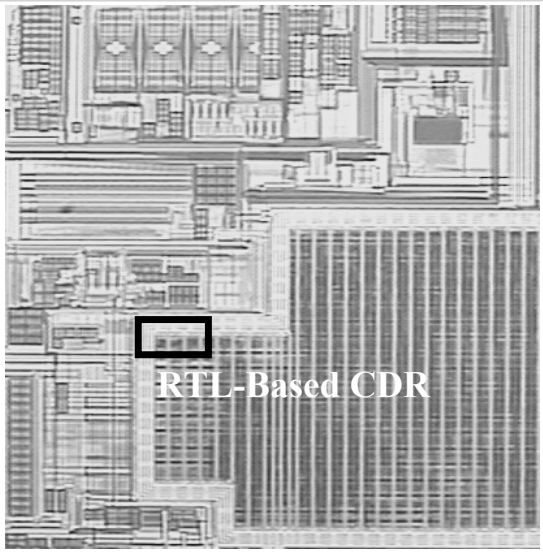

Figure 14.1.7: Die micrograph.

